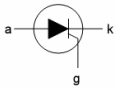
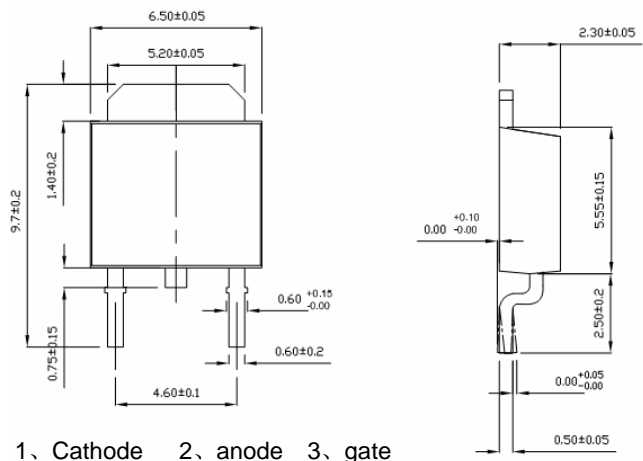


X0405

Thyristors



DRAWING



Mechanical Data

- * TO-252 Package
- * Glass passivated thyristors in a plastic envelope, Intended for use in applications requiring high Bidirectional blocking voltage capability and high Thermal cycling performance. Typical applications Include motor control , industrial and domestic lighting, heating and static switching.

Absolute Ratings (Limiting values)

SYMBOL	PARAMETER			Value	UNIT
$I_{T(RMS)}$	RMS on-state current (180°C conduction angel)		TI=60°C	4	A
			Tamb=25°C	1.35	
$I_{T(AV)}$	Average on-state current(180°C conduction angel)		TI=60°C	2.5	A
			Tamb=25°C	0.9	
I_{TSM}	Non repetitive surge peak on-state current	tp=8.3ms		33	A
		tp=10ms	Tj=25°C	30	
I_t	It Value for fusing	tp=10ms	Tj=25°C	4.5	A ² S
Di/Dt	Critical rate of rise of on-state current $I_g=2XI_{GT, TR} \leq 100ns$	F=60HZ	Tj=125°C	50	A/us
I_{GM}	Peak gate current	tp=20us	Tj=125°C	1.2	A
Pg(AV)	Average gate power dissipation		Tj=125°C	0.2	W
Tstg	Storage junction temperature range			-40to+150	°C
Tj	Operating junction temperature range			-40to+125	

Electrical Characteristics (T_j=25°C, unless otherwise specified)

SYMBOL	Test Conditions		Spec		Unit
IGT			MIN	20	uA
			MAX	50	uA
VGT	VD=12V RL=140Ω		MAX	0.8	V
VGD	VD=VDRM RL=3.3KΩ RGK=1KΩ	TJ=125°C	MIN	0.1	V
VRG	IRG=10uA		MIN	8	V
I _h	I _t =50mA RGK=1KΩ		MAX	5	mA
IL	IG=1mA RGK=1KΩ		MIN	6	mA
DV/DT	VD=67%VDRM RGK=1KΩ	TJ=110°C	MIN	15	V/us
V _{TM}	ITM=8A t _p =380us	TJ=25°C	MAX	1.8	V
V _{to}	Threshold voltage	TJ=125°C	MAX	0.95	V
R _d	Dynamic resistance	TJ=125°C	MAX	100	mΩ
IDRM	VDRM=VRRM RGK=1KΩ	TJ=25°C	MAX	5	uA
IRRM		TJ=125°C		1	mA

Thermal Resistances

SYMBOL	PARAMETER	Value	Unit
R _{th(j-l)}	Junction to leads(DC)	15	°C/W
R _{th(j-a)}	Junction to ambient(DC)	100	

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Fig. 1: Maximum average power dissipation versus average on-state current.

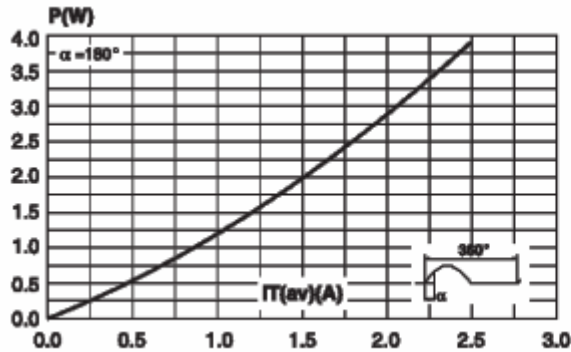


Fig. 2-1: Average and D.C. on-state current versus lead temperature.

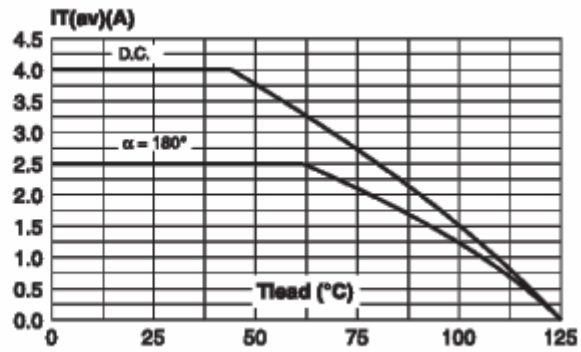


Fig. 2-2: Average and D.C. on-state current versus ambient temperature (device mounted on FR4 with recommended pad layout).

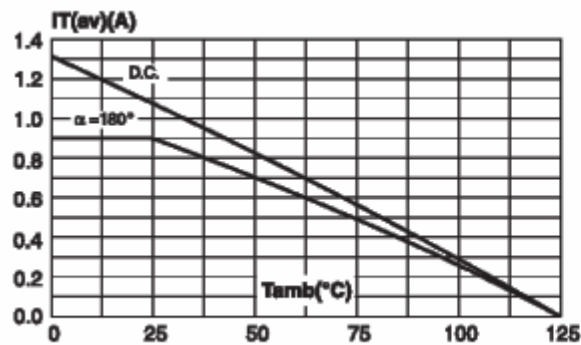


Fig. 3: Relative variation of thermal impedance junction to ambient versus pulse duration.

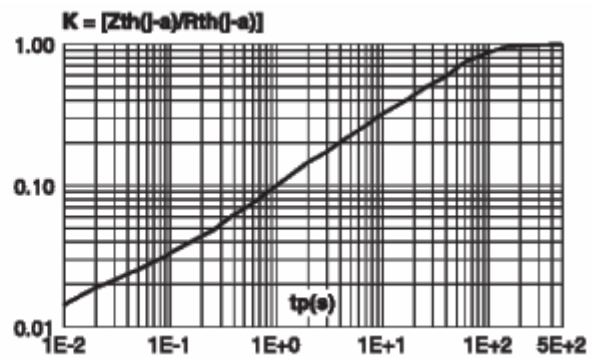


Fig. 4: Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values).

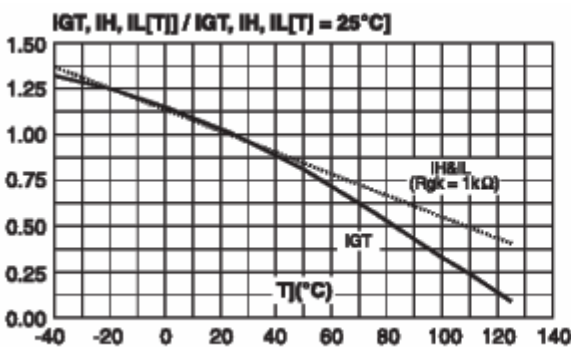


Fig. 5: Relative variation of holding current versus gate-cathode resistance (typical values).

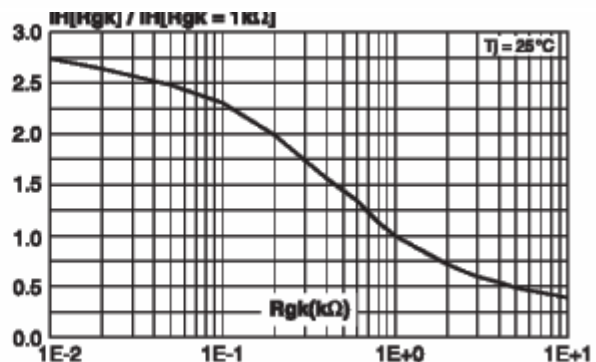


Fig. 6: Relative variation of dV/dt immunity versus gate-cathode resistance (typical values).

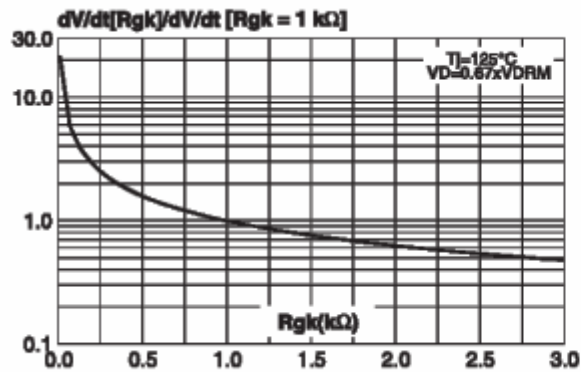


Fig. 7: Relative variation of dV/dt immunity versus gate-cathode capacitance (typical values).

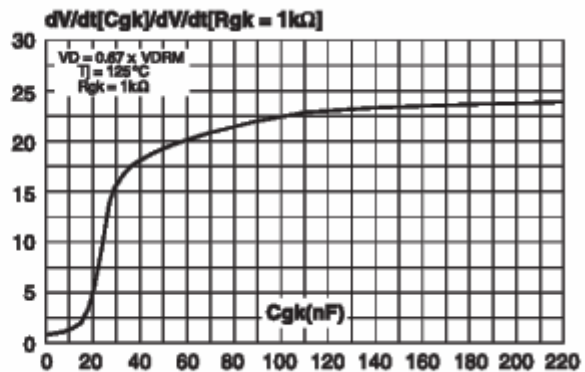


Fig. 8: Surge peak on-state current versus number of cycles.

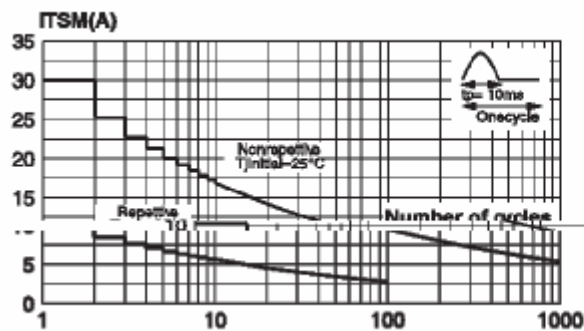


Fig. 9: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $tp < 10$ ms, and corresponding value of $I t$.

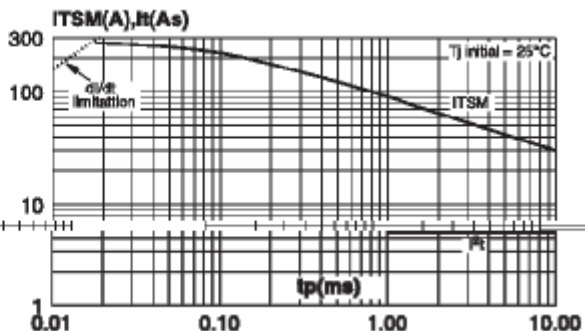


Fig. 10: On-state characteristics (maximum values).

