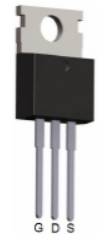
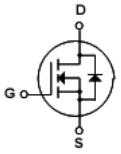
TS75N09

90A 71V N-Channel Enhancement Mode Power Mosfet

DRAWING





Features

- 90A,71V,R_{DSON}=6.8mΩ@V_{GS}=10V
- Special process technology for high ESD capability
- High density cell design for ultra low Rdson
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high Eas
- Excellent package for good heart dissipation

General Description

- Package:TO-220C
- The TS75N09 uses advanced trench technology and design to provide excellent T_{dson} with low gate charge.It can be used in a wide variety of applications.

Absolute Maximum Ratings(Tc=25℃ unless otherwise noted)

Symbol	Parameter	Spec	Units
V_{DSS}	Drain-Source Voltage	71	V
I_D	Drain Current -Continuous(Tc=25℃)	90	A
I_D	Drain Current -Continuous(Tc=100℃)	63	A
I_{DM}	Drain Current -Pulsed	320	A
V_{GSS}	Gate-Source Voltage	±20	V
P_D	Maximum Power Dissipation	160	W
	Derating factor	1.07	w/℃
E_{AS}	Single Pulsed Avalanche Energy (Note 5)	550	mJ
T_J.T_{DTG}	Operating Junction and Storage Temperature Range	-55 to +175	℃
R_{JC}	Thermal Resistance,Junction-to-Case (Note 2)	0.94	℃/W

Electrical Characteristics(Tc=25℃ unless otherwise noted)

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V,I_D=250uA	71	74	_	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=65V,V_{GS}=0V	_	_	1	uA
I_{GSS}	Gate-Body Leakage Current,	Vgs=±20V,Vds=0V	_	_	±100	nA

On Characteristics (Note 3)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{GSTH}	Gate Threshold Voltage	VDS=VGS,ID=250uA	2.0	3.0	4.0	V
R_{DSON}	Static Drain-Source On-Resistance	VGS=10V,ID=40A	_	5.9	6.8	mΩ
g_{FS}	Forward Transconductance	VDS=5V,ID=40A	60	-	-	S

Dynamic Characteristics (Note 4)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Cjss	Input Capacitance	VDS=30V,VGS=0V,f=1.0MHz	_	4800		pF
Coss	Output Capacitance		_	440		pF
Crss	Reverse Transfer Capacitance		_	260		pF

Switching Characteristics (Note 4)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{don}	Turn-On Delay Time	V_{DD}=30V	_	16.8	_	ns
t_r	Turn-On Rise Time	I_D=1A	_	10.8	_	ns
t_{doff}	Turn-Off Delay Time	R_G=2.5Ω	_	55	_	ns
t_f	Turn-Off Fall Time	VGS=10V	_	13.6	_	ns
Q_g	Total Gate Charge	V_{DS}=30V	_	85	_	nc
Q_{gs}	Gate-Source Charge	I_D=30A	_	18	_	nc
Q_{gd}	Gate-Drain Charge	V_{GS}=10V	_	28	_	nc

Drain-Source Diode Characteristics and Maximum Ratings

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Is	diode forward current (Note 3)		_	_	90	A
Vsd	diode forward Voltage (Note 2)	VGS=0V,IS=20A	_	_	1.2	V
Trr	Reverse Recovery Time	TJ=25℃,IS=40A	_	38	_	ns
Qrr	Reverse Recovery charge	dif/dt=100A/us (Note 3)	_	53	_	uc
T_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible(turn-on is dominated by LS+LD)				

Notes:

1.Repetitive Rating: Pulse width limited by maximum junction temperature.

2.Surface Mounted on FR4 Board, t≤10 sec

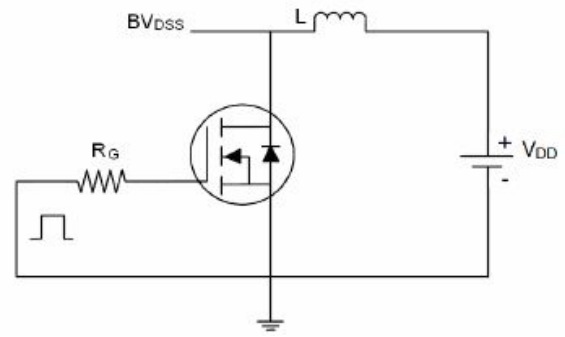
3.Pulse Test: Pulse Width ≤300us,Duty cycle≤2%

4.Guaranteed by design, not subject to production

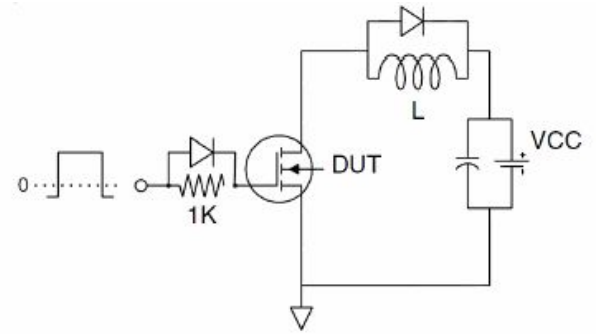
5.EAS condition: Tj=25℃,VDD=30V,VG=10V,L=0.5mH,Rg=25Ω

Test circuits

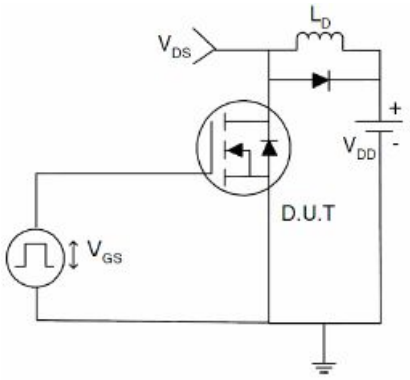
1)EAS Test Circuits



2)Cate Charge Test Circuit



3）Switch Time Test Circuit



Typical Electrical And Thermal Characteristics(Curves)

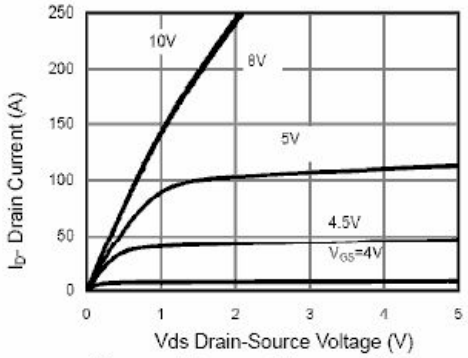


Figure 1 Output Characteristics

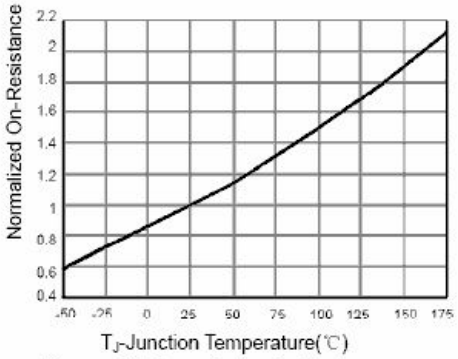


Figure 4 Rdson-JunctionTemperature

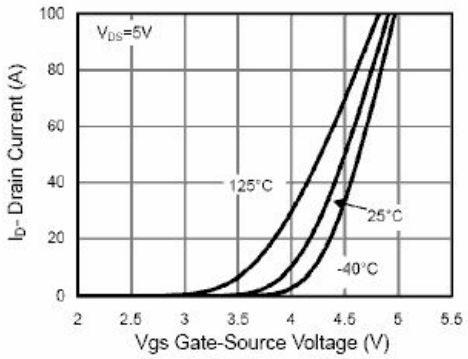


Figure 2 Transfer Characteristics

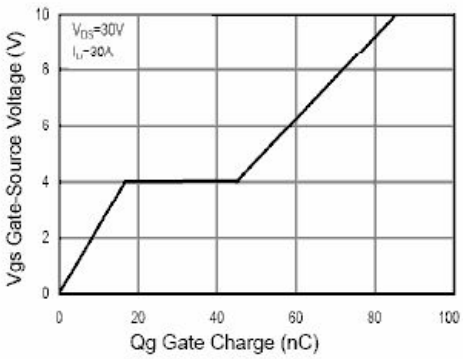


Figure 5 Gate Charge

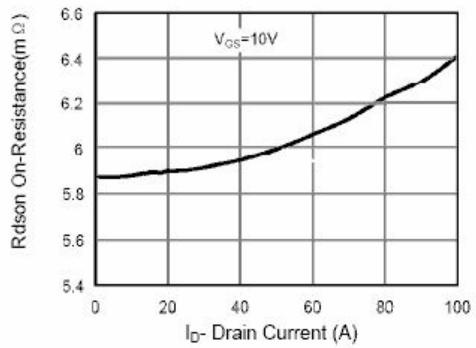


Figure 3 Rdson- Drain Current

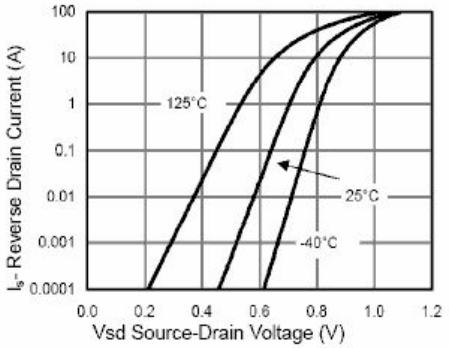


Figure 6 Source- Drain Diode Forward

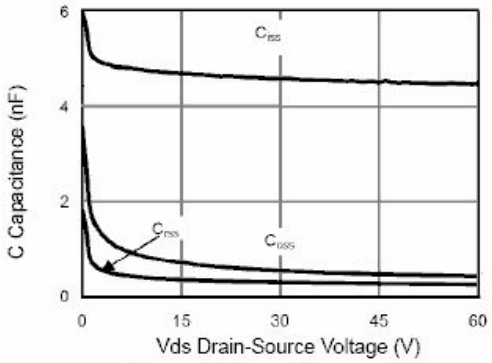


Figure 7 Capacitance vs Vds

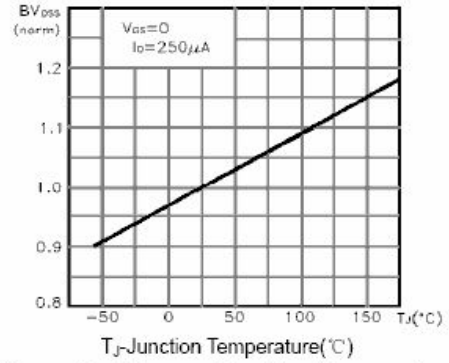


Figure 9 BV_{DSS} vs Junction Temperature

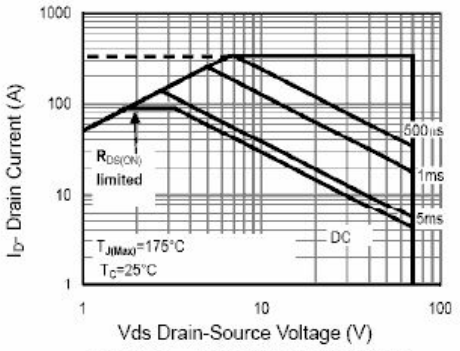


Figure 8 Safe Operation Area

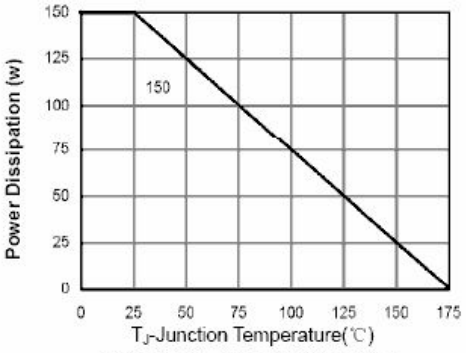


Figure 10 Power De-rating

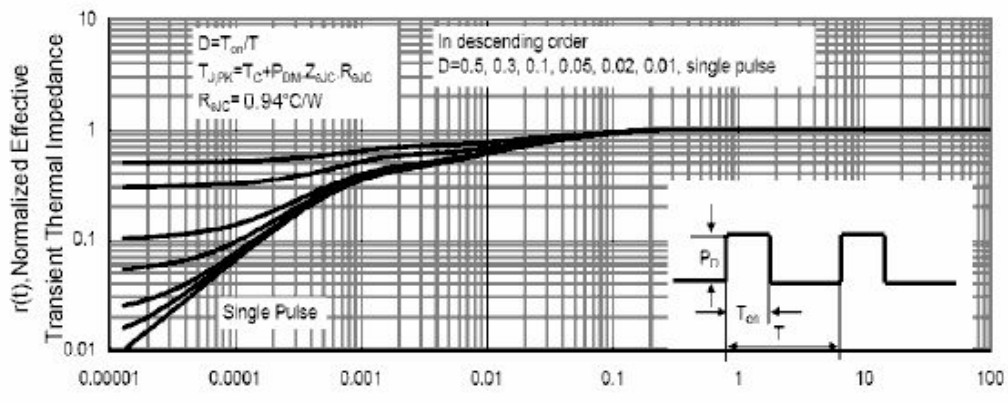


Figure 11 Normalized Maximum Transient Thermal Impedance

Mechanical Dimensions