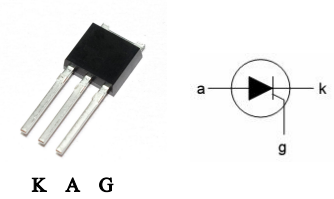
BT152

Thyristors

DRAWING



General Description

- Package: TO-251A
- Glass passivated thyristors in a plastic envelope,Intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance.Typical applications include motor control ,industrial and domestic lighting,heating and static switching.

Limiting Values

Limiting values in accordance with the absolute Maximum System(IEC134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DRM},V_{RRM}	Repetitive peak off-state Voltages			600	V
$I_{T(AV)}$	Average on-state current	half sine wave;Tmb≤109℃		13	A
$I_{T(RMS)}$	RMS on-state current	all conduction angles		20	A
I_{TSM}	Non-repetitive peak on-state current	half sine wave;Tj=25℃ prior to surge			
		t=10ms		200	A
		t=8.3ms		220	A
I^2T	I^2T for fusing	t=10ms		200	A^2S
Dit/dt	Repetitive rate of rise of on-state current after triggering	I_{TM}=20A;IG=50mA;Dig/dt=50mA/us		200	A/us
I_{GM}	Peak gate current			5	A
Vgm	Peak gate voltage			5	V
V_{RGM}	Peak reverse gate voltage			5	V
P_{GM}	Peak gate power			20	W
$P_{G(AV)}$	Average gate power	over any 20 ms period		0.5	W
T_{STG}	Storage temperature		-40	150	℃
Tj	Operating junction temperature			125	℃

Thermal Resistances

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Rthj-mb	Thermal resistance junction to mounting base				1.8	K/W
Rthj-a	Thermal resistance junction to ambient			75		K/W

Static Characteristics(Tj=25℃ unless otherwise stated)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{GT}	Gate trigger current	V_D=12V;I_T=0.1A		3	32	mA
I_L	Latching current	V_D=12V;I_{GT}=0.1A		25	80	mA
I_H	Holding current	V_D=12V;I_{GT}=0.1A		15	60	mA
V_T	On-state voltage	I_T=23A		1.4	1.75	V
V_{GT}	Gate trigger voltage	V_D=12V;I_T=0.1A		0.6	1.5	V
		V_D=$V_{DRM(MAX)}$;I_T=0.1A;T_J=125℃	0.25	0.4		V
I_D,I_R	Off-state leakage current	V_D=$V_{DRM(MAX)}$;V_R=$V_{RRM(MAX)}$;TJ=125℃		0.2	1.0	mA

Dynamic Characteristics(Tj=25℃ unless otherwise stated)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
DVD/dt	Critical rate of rise or off-state voltage	VDM=67%VDRM(MAX);TJ=125℃; exponential waveform Gate open circuit	200	300		V/us
tgt	Gate controlled turn-on time	ITM=40A;VD=VDRM(MAX);IG=0.1A		2		us
		Dig/dt=5A/us				
tq	Circuit commutated turn-off time	VD=67%VDRM(MAX);TJ=125℃		70		us
		ITM=20A;VR=25V;Ditm/dt=30A/us				
		dvd/dt=50V/us;Rgk=100Ω				

Typical Characteristics

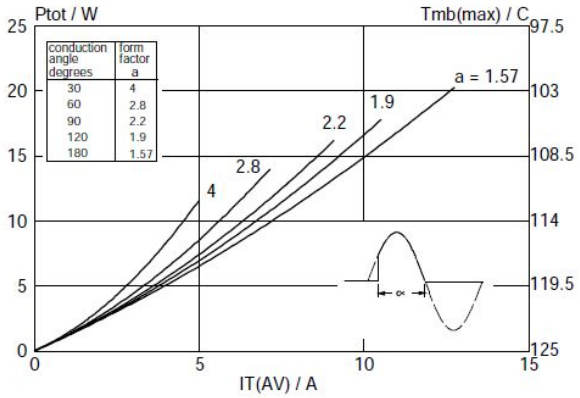


Fig.1. Maximum on-state dissipation, P_{tot}, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}$/ $I_{T(AV)}$.

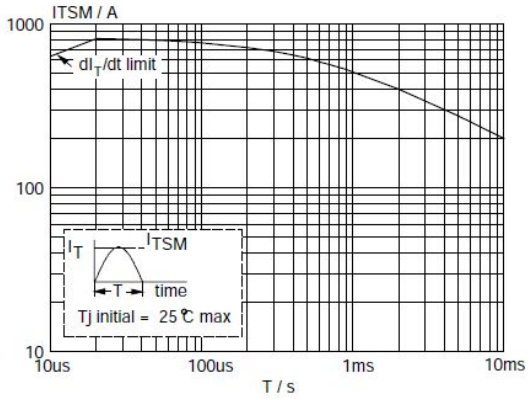


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 10ms$.

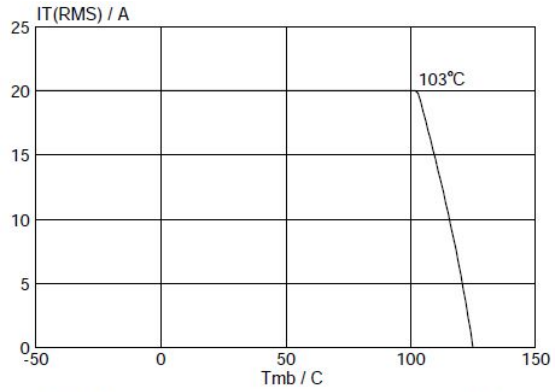


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

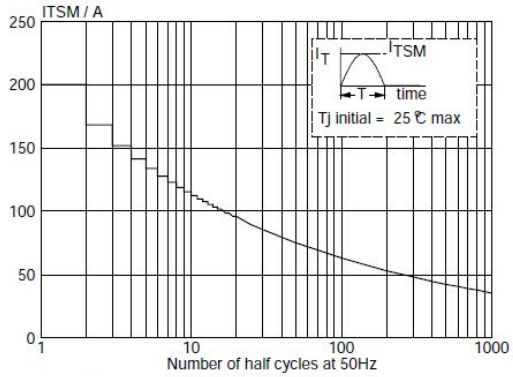


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

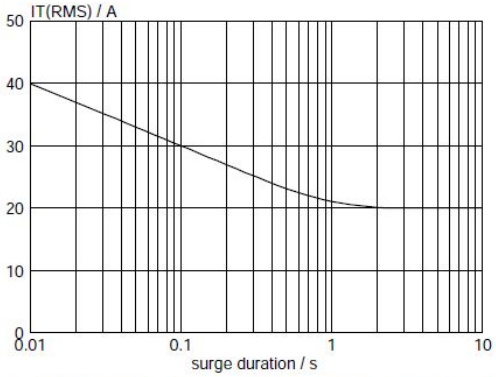


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 103^{\circ}C$.

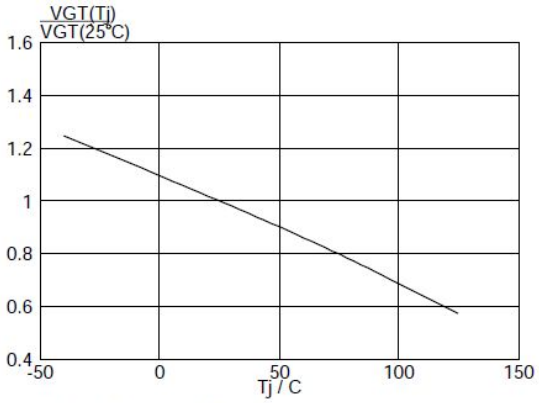


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25^{\circ}C)$, versus junction temperature T_j.

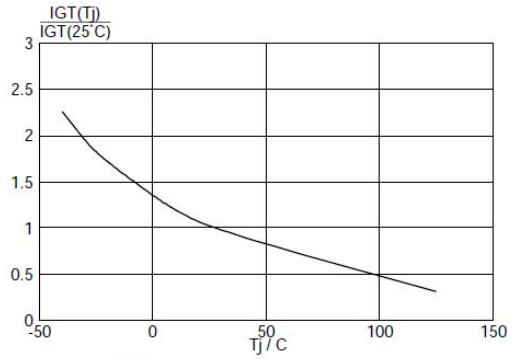


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25^{\circ}C)$, versus junction temperature T_j.

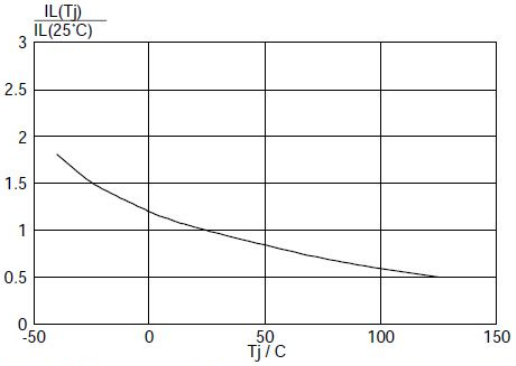


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25^{\circ}C)$, versus junction temperature T_j.

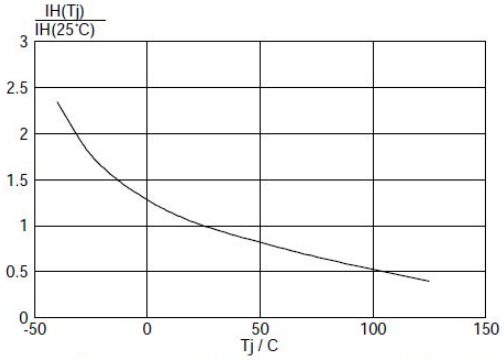


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25^{\circ}C)$, versus junction temperature T_j.

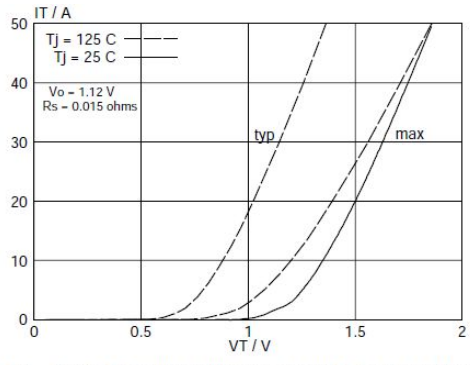


Fig.10. Typical and maximum on-state characteristic.

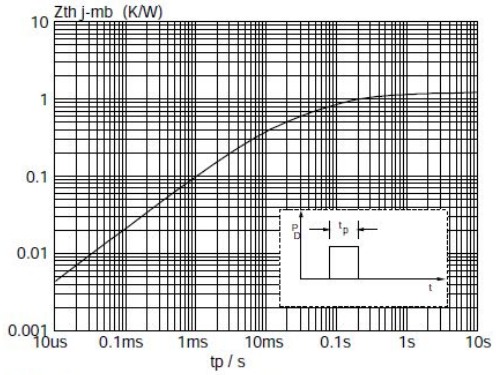


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$ versus pulse width t_p.

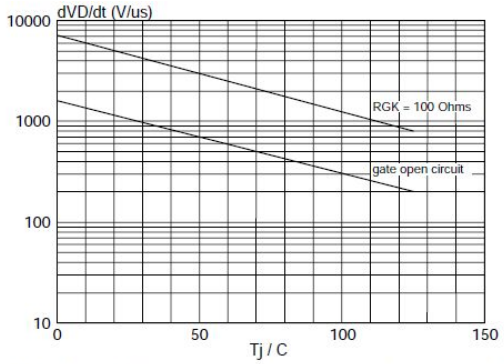


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

Mechanical Dimensions