

TS01N100

N-Channel Enhancement Mode Power Mosfet

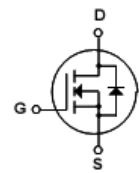
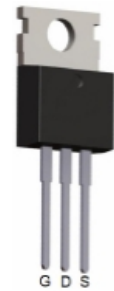
DRAWING

Features

- ◆ $V_{DS}=100V, I_D=100A,$
 $R_{DS(ON)} < 11m\Omega @ V_{GS}=10V (TYPE: 9.9m\Omega)$
- ◆ Special process technology for high ESD capability
- ◆ High density cell design for ultra low Rdson
- ◆ Fully characterized avalanche voltage and current
- ◆ Good stability and uniformity with high E_{AS}
- ◆ Excellent package for good heat dissipation

Description

- ◆ Package: TO-220C
- ◆ The TS01N100 uses advanced trench technology and design to provide excellent RDS(ON) with low gate charge. It can be used in a wide variety of applications.



Absolute Maximum Ratings

Symbol	Parameter	Limit	Unit
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current -Continuous($T_c=25^\circ C$)	100	A
$I_D(100^\circ C)$	Drain Current -Continuous($T_c=100^\circ C$)	80	A
I_{DM}	Pulsed Drain Current	380	A
P_D	Maximum Power Dissipation	200	W
	Derating factor	1.33	W/ $^\circ C$
E_{AS}	Single pulse Avalanche Energy(Note5)	800	mJ
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	$^\circ C$

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Ambient(Note2)	-	0.75	$^\circ C/W$

Electrical Characteristics($T_c=25^\circ C$ unless otherwise noted)

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100	110	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=100V, V_{GS}=0V$	-	-	1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA

On Characteristics(Note 3)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	$V_{GS}=10V, I_D=40A$	—	9.9	13	m Ω
g_{FS}	Forward Transconductance	$V_{DS}=50V, I_D=40A$	100	-	-	S

Dynamic Characteristics(Note 4)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
C_{iss}	Input Capacitance	$V_{DS}=50V, V_{GS}=0V, F=1.0MHz$	—	4800	—	PF
C_{oss}	Output Capacitance		—	340	—	
C_{rss}	Reverse Transfer Capacitance		—	150	—	

Switching Characteristics(Note 4)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-On Delay Time	$V_{DD}=50V, I_D=40A$ $V_{GS}=10V, R_{GEN}=2.5\Omega$	—	15	—	ns
t_r	Turn-On Rise Time		—	50	—	ns
$t_{d(off)}$	Turn-Off Delay Time		—	40	—	ns
t_f	Turn-Off Fall Time		—	55	—	ns
Q_g	Total Gate Charge	$V_{DS}=80V$	—	85	—	nc
Q_{gs}	Gate-Source Charge	$I_D=40A$	—	18	—	nc
Q_{gd}	Gate-Drain Charge	$V_{GS}=10V$	—	28	—	nc

Drain-Source Diode Characteristics

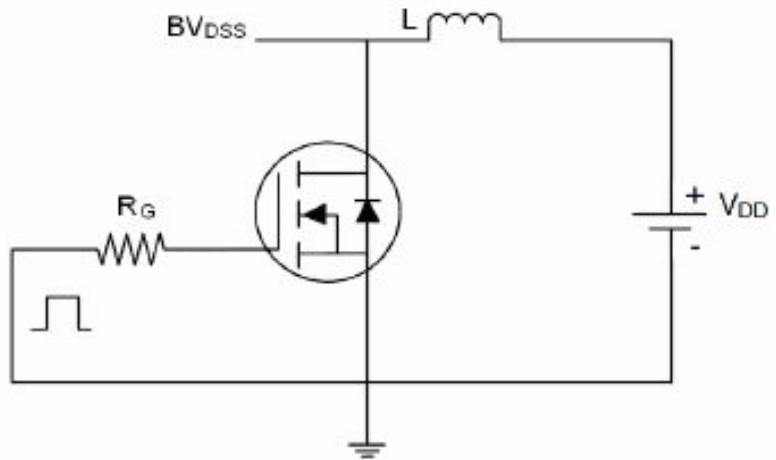
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_S	Diode forward current(Note 2)		—	—	57	A
V_{SD}	Diode Forward Voltage(Note 3)	$V_{GS}=0V, I_S=40A$	—	—	1.2	V
t_{rr}	Reverse Recovery Time	$T_J=25^\circ C, I_F=40A$	—	38	80	ns
Q_{rr}	Reverse Recovery charge	$diff/dt=100A/\mu s$ (Note 3)	—	53	100	nc
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible(Turn-on is dominated by LS+LD)				

Notes:

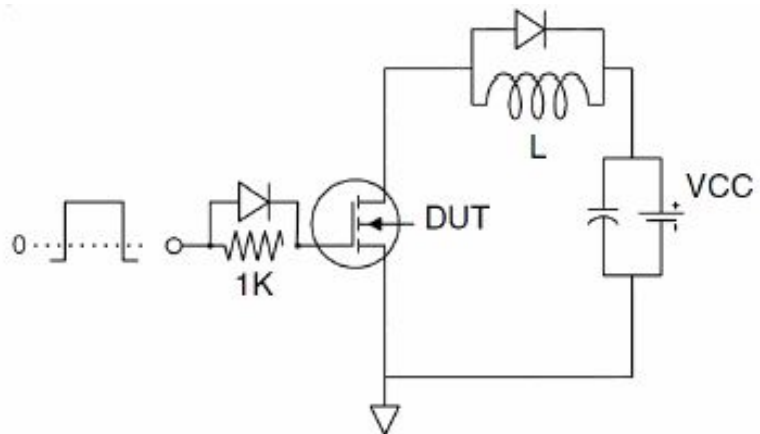
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^\circ C, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test circuits

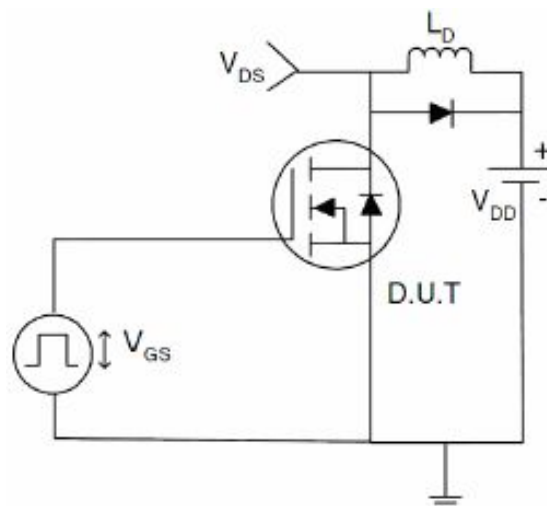
1)EAS Test Circuits



2)Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical And Thermal Characteristics(Curves)

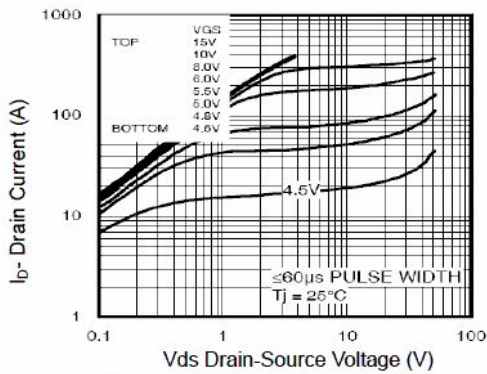


Figure 1 Output Characteristics

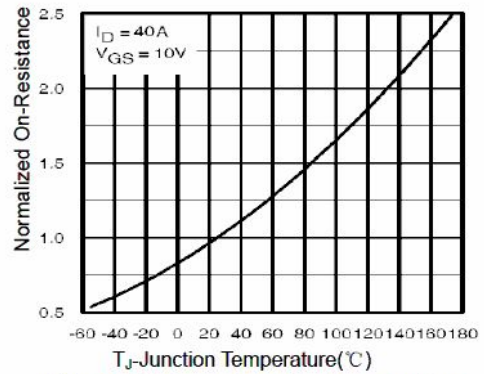


Figure 4 Rdson-Junction Temperature

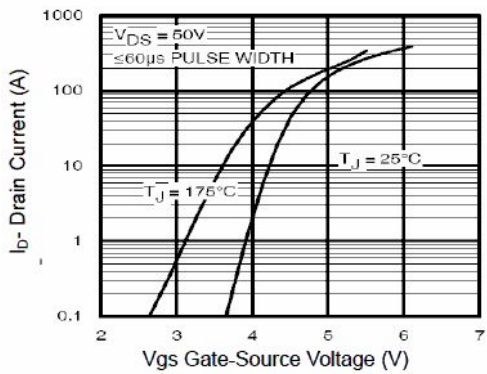


Figure 2 Transfer Characteristics

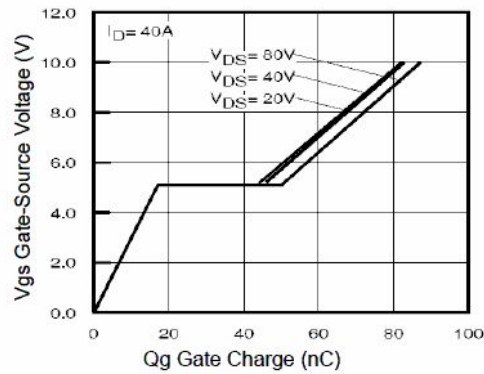


Figure 5 Gate Charge

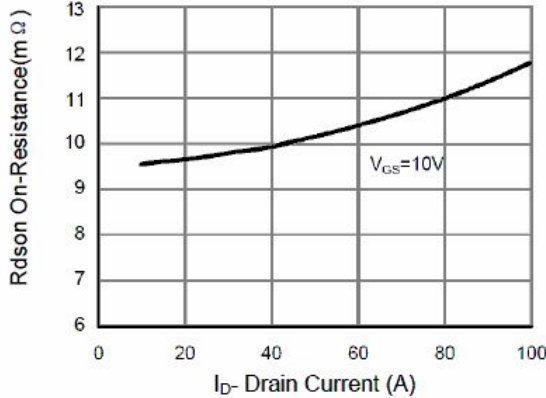


Figure 3 Rdson- Drain Current

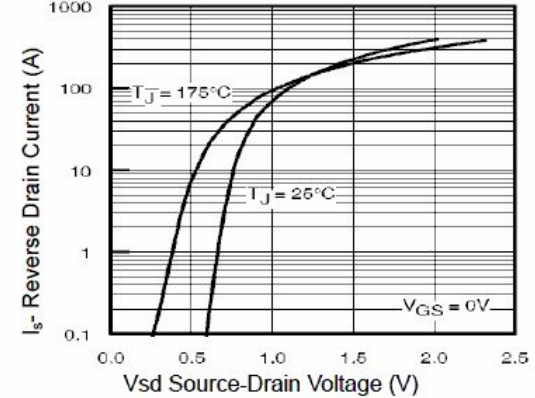


Figure 6 Source- Drain Diode Forward

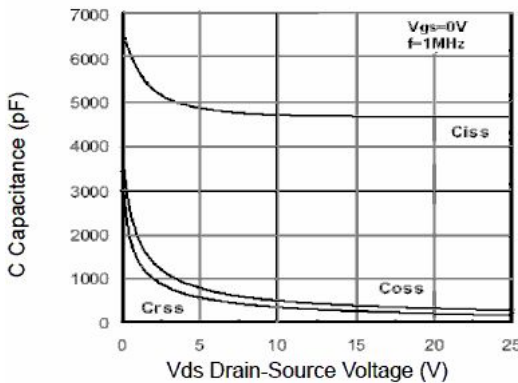


Figure 7 Capacitance vs Vds

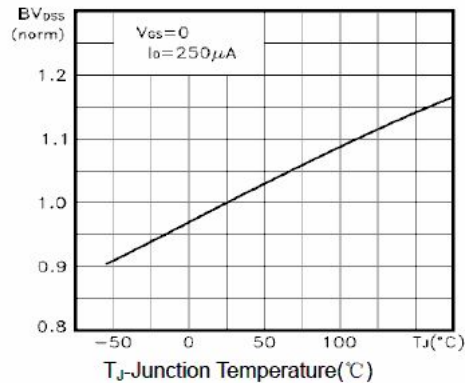


Figure 9 BVdss vs Junction Temperature

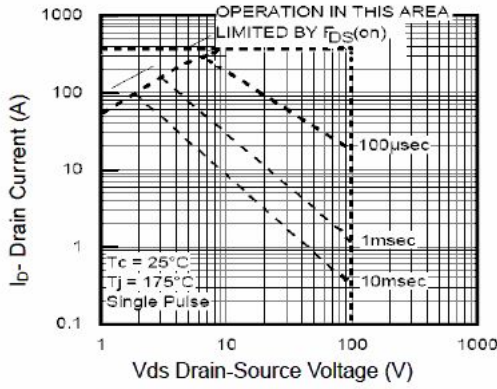


Figure 8 Safe Operation Area

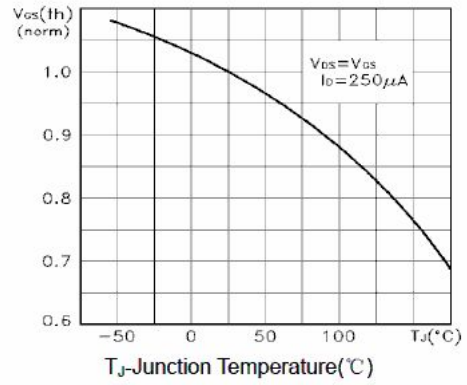


Figure 10 $V_{GS(th)}$ vs Junction Temperature

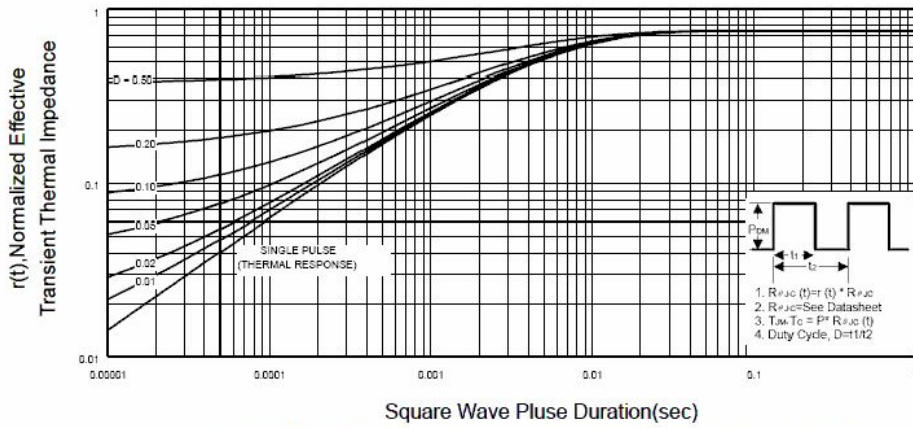


Figure 11 Normalized Maximum Transient Thermal Impedance

Mechanical Dimensions

