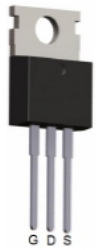
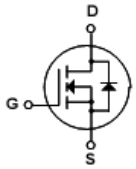
TS150N05

N-Channel Enhancement Mode Power MOSFET

DRAWING





Features

- V_{DS} =150V,I_D =50A, $R_{DS(ON)}$ <23mΩ @ V_{GS}=10V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high EAS
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

General Description

- Package:TO-220C
- The TS150N05 uses advanced trench technology and design to provide excellent RDS(ON) with low gate charge. It can be used in a wide variety of applications.

Application

- Power switching application
- Hard switched and High frequency circuits
- Uninterruptible power supply

Absolute Maximum Ratings

Symbol	Parameter	Spec	Units
V_{DS}	Drain-Source Voltage	150	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Drain Current -Continuous(Tc=25℃)	50	A
I_D	Drain Current -Continuous(Tc=100℃)	35	A
I_{DM}	Pulsed Drain Current	210	A
P_D	Maximum Power Dissipation	220	W
	Derating factor	1.47	W/℃
E_{AS}	Single pulse avalanche energy (Note 5)	640	mJ
T_J,T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	℃

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case(Note 2)	_	0.68	℃/W

Electrical Characteristics(Tc=25℃ unless otherwise noted)

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V,I_D=250uA	150	170		V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=100V,V_{GS}=0V			1	uA
I_{GSS}	Gate-Body Leakage Current	Vgs=±20V,Vds=0V			±100	nA

On Characteristics(Note 3)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=VGS,I_D=250uA	2.5	3.2	4.5	V
R_{DSON}	Static Drain-Source On-Resistance	V_{GS}=10V,I_D=40A		19.5	23	mΩ
g_{FS}	Forward Transconductance	V_{DS}=25V,I_D=30A	85			S

Dynamic Characteristics(Note 4)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Cjss	Input Capacitance	V_{DS}=25V,V_{GS}=0V,f=1.0MH_Z		3250		pF
Coss	Output Capacitance			670		pF
Crss	Reverse Transfer Capacitance			150		pF

Switching Characteristics(Note 4)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{don}	Turn-On Delay Time	V_{DD}=30V, I_D=2A, R_L=15Ω V_{GS}=10V, R_G=2.5Ω		26		ns
t_r	Turn-On Rise Time			24		ns
t_{doff}	Turn-Off Delay Time			91		ns
t_f	Turn-Off Fall Time			39		ns
Q_g	Total Gate Charge	V_{DS}=30V,I_D=30A, V_{GS}=10V		163		nc
Q_{gs}	Gate-Source Charge			31		nc
Q_{gd}	Gate-Drain Charge			64		nc

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Vs	Diode Forward Voltage (Note 3)				1.2	V
Is	Diode Forward Current(Note 2)				50	A
Trr	Reverse Recovery Time	Tj=25℃,IF=40A, dif/dt=100A/us (Note 3)		42		ns
Qrr	Reverse Recovery charge			66		uc
ton	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

2. Surface Mounted on FR4 Board, t ≤ 10 sec.

3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

4. Guaranteed by design, not subject to production

5. EAS condition: Tj=25℃,VDD=50V,VG=10V,L=0.5mH,Rg=25Ω

Typical Characteristics

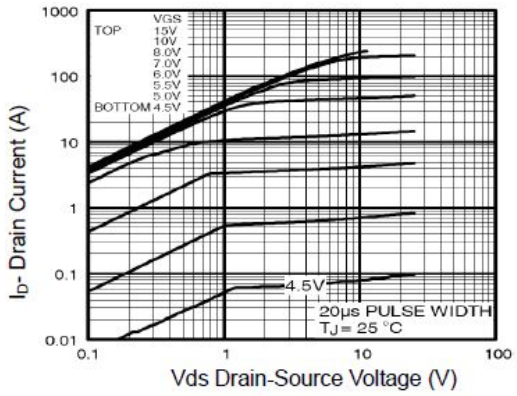


Figure1. Output Characteristics

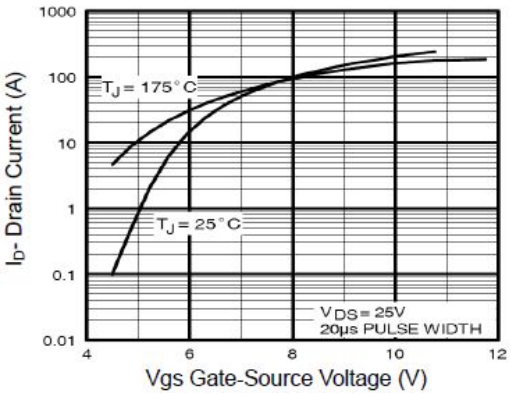


Figure2. Transfer Characteristics

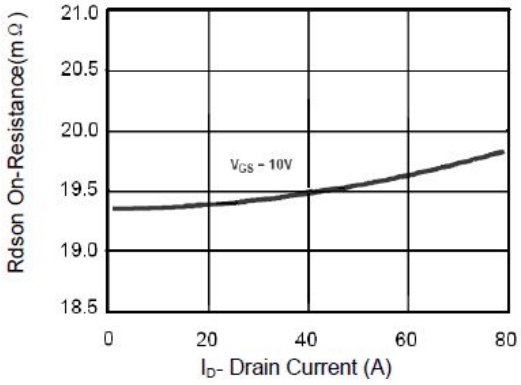


Figure3. Rdson-Drain current

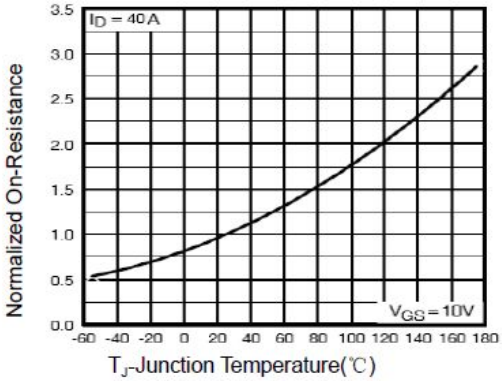


Figure4. Rdson-Junction Temperature

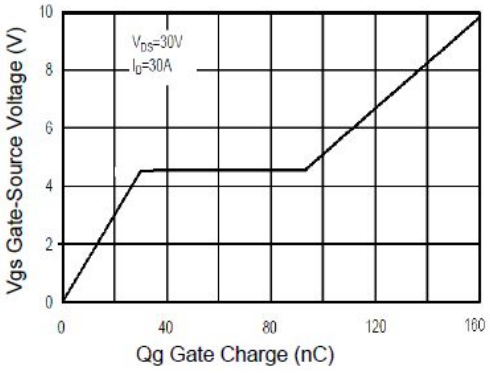


Figure5. Gate Charge

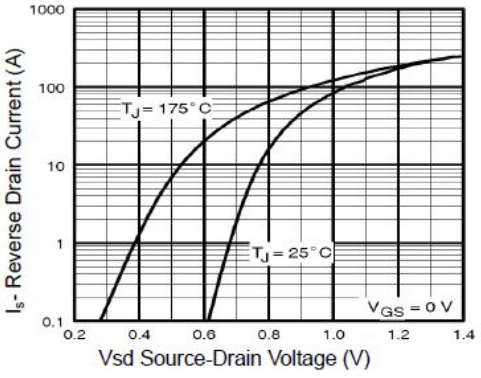


Figure6. Source- Drain Diode Forward

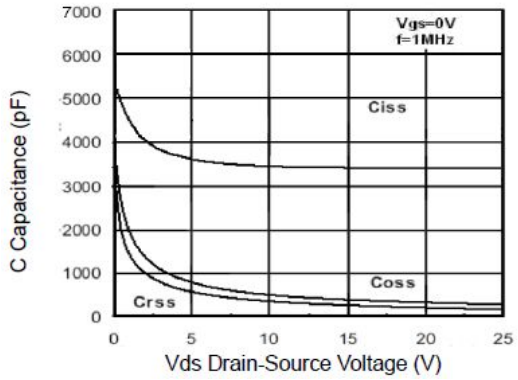


Figure7. Capacitance vs Vds

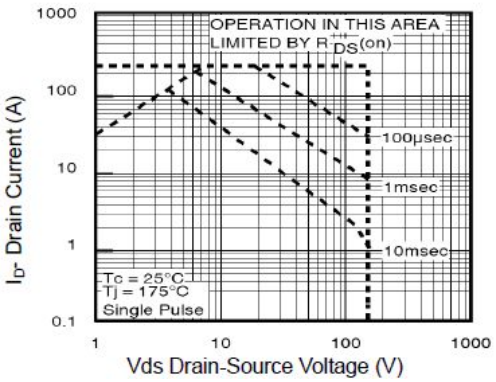


Figure8. Safe Operation Area

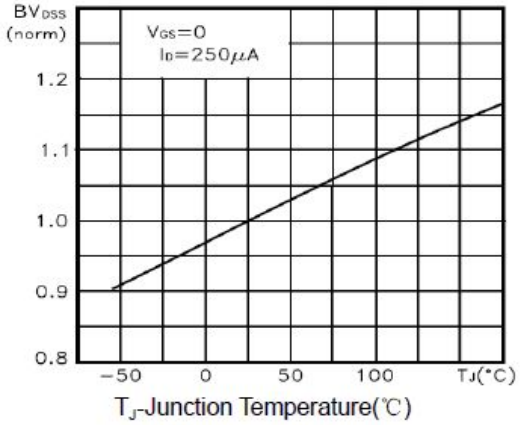


Figure9. BVDSS vs Junction Temperature

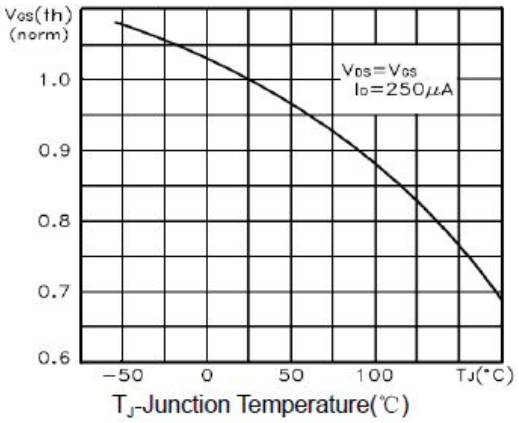


Figure10. VGS(th)s vs Junction Temperature

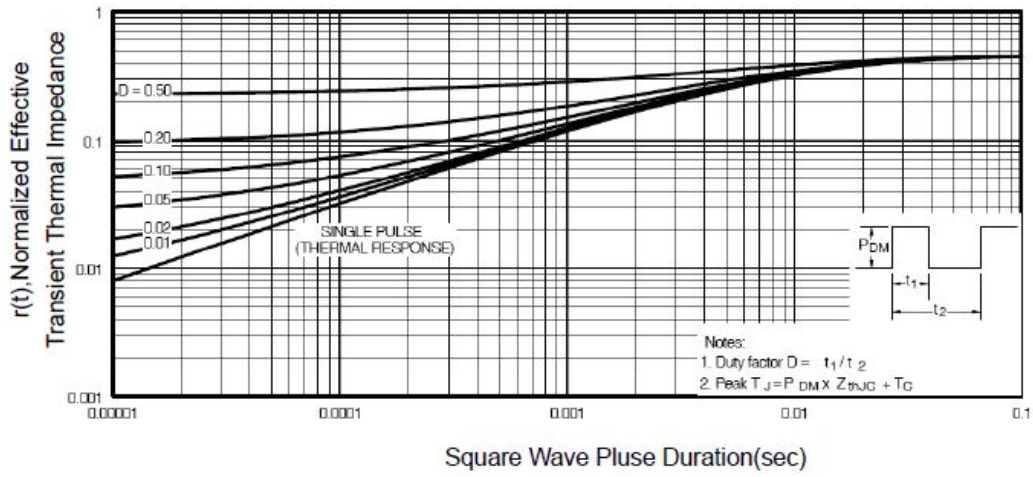
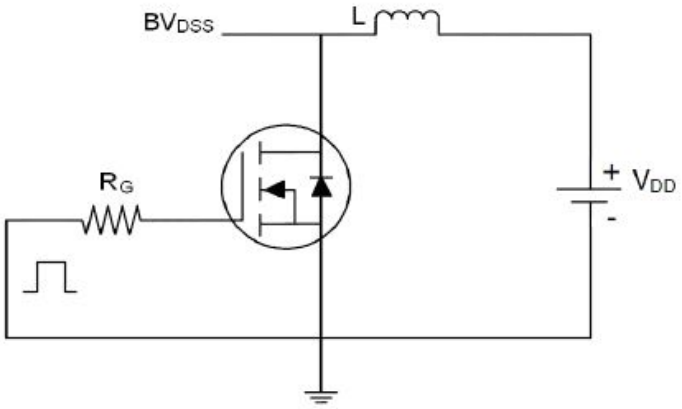


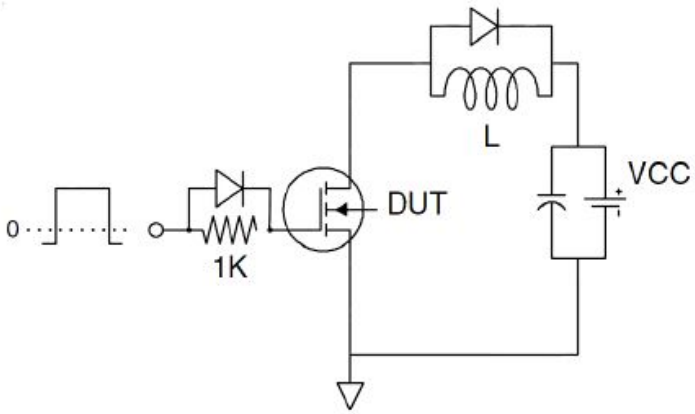
Figure11. Normalized Maximum Transient Thermal Impedance

Test Circuits

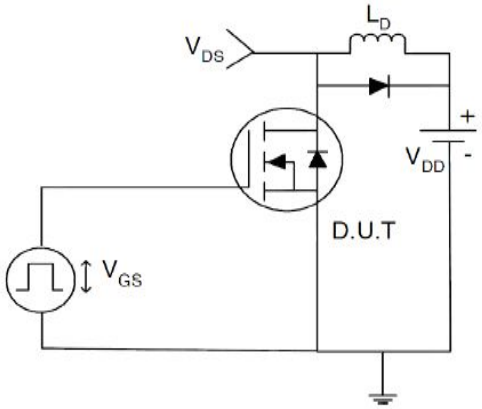
1)EAS Test Circuit



2)Gate Charge Test Circuit



3)Switch Time Test Circuit



Mechanical Dimensions